

15 kV-Class Implantation-Free 4H-SiC BJTs With Record High Current Gain

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Abstract—Implantation-free mesa-etched ultra-high-voltage (0.08 mm^2) 4H-SiC bipolar junction transistors (BJTs) with record current gain of 139 are fabricated, measured, and analyzed by device simulation. High current gain is achieved by optimized surface passivation and optimal cell geometries. The area-optimized junction termination extension is utilized to obtain a high and stable breakdown voltage without ion implantation. The open-base blocking voltage of 15.8 kV at a leakage current density of 0.1 mA/cm^2 is achieved. Different cell geometries (single finger, square, and hexagon cell geometries) are also compared.

Index Terms—Ultra-high-voltage 4H-SiC BJT, implantation-free, area-optimized junction termination extension (O-JTE), current gain, on-resistance, optimal cell geometries, surface passivation.

I. INTRODUCTION

ULTRA-HIGH-VOLTAGE ($>10 \text{ kV}$) bipolar junction transistors (BJTs) based on 4H-SiC are attractive candidates for high-voltage switching due to their excellent characteristics such as low ON-resistance (R_{ON}) at high current density, high breakdown voltage, negative coefficient of the current gain (β), normally-off switching behavior, and absence of gate-oxide reliability problems [1], [2]. Thanks to its high electron saturation velocity and high electric field, there is no reverse-biased second breakdown during turn-off for 4H-SiC BJTs. This results in a large safe operating area [3]. However, improvement of the BJT characteristics such as β plays a key role to effectively compete with metal oxide semiconductor field effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs). Therefore, there has been growing interest in enhancing the 4H-SiC BJT characteristics [3]–[25]. Recently, we reported 42% higher J_C and 21% lower R_{ON} for the hexagon- and square-cell geometries due to a better utilization of the base area [5].

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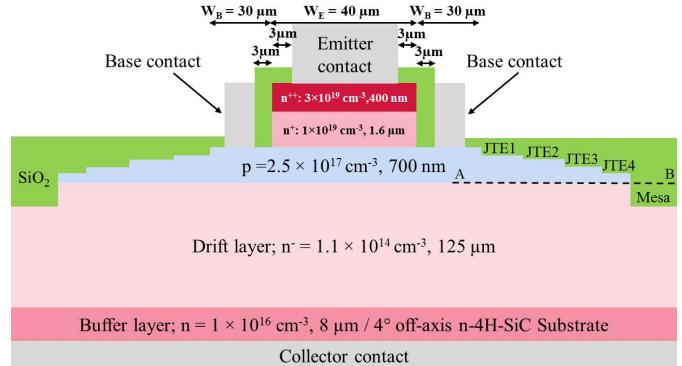


Fig. 1. Schematic cross-sectional view of the fabricated 4H-SiC BJT. The A-B cutline used in the simulation is marked in the cross-section.

To develop SiC BJTs for ultra-high-voltage applications, a proper edge termination is needed to reduce the electric field crowding at the mesa edge. Generally, ion implantation is utilized to form the junction termination extension (JTE). However, ion implantation followed by high-temperature annealing is known to produce lifetime killer defects, resulting in a lower current gain [12], [21]. Only a few reports on SiC high- and ultra-high-voltage BJTs are available; 9.2 kV BJT (0.09 mm^2) with a β of 7 [8], 10 kV BJT (0.336 cm^2) with a β of 28 [26], 10 kV BJT (2.7 and 28 mm^2) with a β of 75 [18], and 21 kV BJT (0.035 mm^2) with a β of 63 [27]. Although high current gain of ($\beta = 257$) has been reported for a low-voltage BJT [7], the β is in the range of 60–75 for high-voltage and ultra-high-voltage BJTs [18], [27]. In this work, we report a significant improvement in the current gain of ($\beta = 139$) in 15 kV-class small-area (0.08 mm^2) 4H-SiC BJTs, utilizing an efficient and optimized implantation-free junction termination extension (O-JTE) [12], [13]. An optimized surface passivation and cell geometry were utilized to achieve a high β , following [11] and [25], respectively. We compare the β for different emitter cell geometries (single finger, square, and hexagon). The base size effect is also investigated.

II. DEVICE FABRICATION

Fig. 1 shows a cross-sectional view of the fabricated 15 kV-class small-area (0.08 mm^2) 4H-SiC single finger BJT with an emitter width (W_E) of $40 \mu\text{m}$ and a base width (W_B) of $30 \mu\text{m}$. An $8\text{-}\mu\text{m}$ thick epitaxial n-type buffer layer was

TABLE I
THE LENGTH AND THE ETCHING DEPTH OF THE O-JTE STRUCTURE

Zone	JTE1	JTE2	JTE3	JTE4	Mesa
Etching depth	260 nm	80 nm	80 nm	120 nm	1.5 μm
Length	350 μm	263 μm	175 μm	87 μm	80 μm

grown and doped to $1.1 \times 10^{16} \text{ cm}^{-3}$ on a 100-mm 4° off-axis 4H-SiC substrate. Then, a 125- μm -thick n^- drift layer was grown and nitrogen doped to $1.1 \times 10^{14} \text{ cm}^{-3}$. The wafer received chemical mechanical polishing (CMP) to improve the surface morphology followed by an epilayer growth of 700 nm thick p-layer aluminum doped to $2.5 \times 10^{17} \text{ cm}^{-3}$. Finally, a n^+ -emitter epilayer 1.6 μm thick, and nitrogen doped to $1 \times 10^{19} \text{ cm}^{-3}$ was grown and capped by a 400-nm-thick $3 \times 10^{19} \text{ cm}^{-3}$ epilayer to obtain optimum injection efficiency and low-resistive ohmic contact, respectively. An O-JTE structure with a descending length of the JTE zones was applied to achieve a lower peak and uniform electric field distribution. Three main parameters were optimized to achieve the optimum design (see Table I); the number of the JTE zones, their etching depth, and their lengths according to [12]. The device design allows for a theoretical breakdown voltage of about 19 kV according to Sentaurus TCAD simulations. Reactive ion etching (RIE) with a photoresist mask was utilized to form a well-controlled four-zone etched JTE. To achieve a precisely etch depth, firstly, the SiC etch rate was measured and then each zone was etched in several steps. The etch depth of all steps were measured utilizing a profilometer. Inductively coupled plasma (ICP) etching with an oxide mask was used to form the emitter and final mesa.

A dry sacrificial oxidation process was performed for 3 hours at 1100 °C to reduce the surface defects caused by the etching steps according to [28]. A surface passivation was grown using 100-nm plasma enhanced chemical vapor deposited (PECVD) SiO_2 followed by post-deposition annealing in N_2O ambient at 1250 °C for 1 hour to minimize the interface charges at the SiO_2/SiC interface, following [11]. A 70-nm and 140-nm Ni layer were deposited for emitter and collector contacts respectively. Rapid thermal annealing (RTA) was done at 950 °C for 1 min in N_2 ambient to form the ohmic n-contact. A 110-nm stack layer of Ni/Ti/Al was deposited with the thickness of 10/15/85 nm for the base contacts. To form the ohmic p-contact, RTA was done at 850 °C for 90 sec in Ar ambient. Utilizing transmission line method (TLM) structures, the emitter, and base contact resistivities were extracted to $1.6 \times 10^{-6} \Omega \cdot \text{cm}^2$ and $1.8 \times 10^{-3} \Omega \cdot \text{cm}^2$ respectively. The intrinsic base sheet resistance was extracted to 38 k Ω/sq . A 500-nm thick Al layer was sputtered on the emitter and base contacts for current spreading. Subsequently, a 2.5- μm thick SiO_2 layer was deposited by PECVD. Contact windows were then opened in the oxide and a 3- μm Al layer was sputtered and formed on the emitter and base. Finally, a 450-nm stack of TiW/Ni/Au was sputter deposited with a thickness ratio of 50/300/100 nm for the backside collector contact.

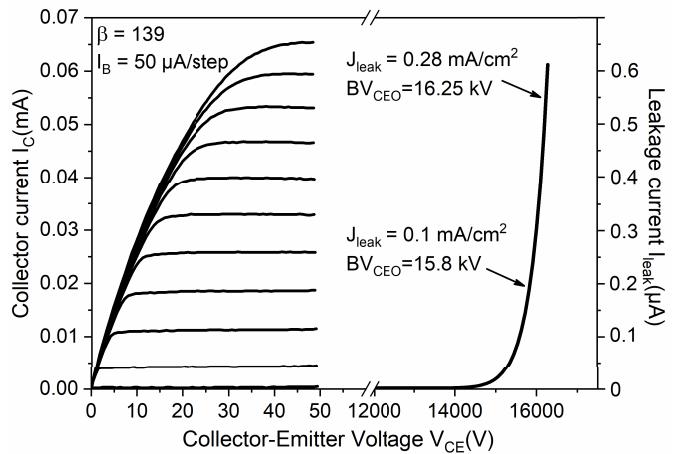


Fig. 2. Room temperature I - V characteristics of the fabricated 0.08 mm^2 (active area of 0.18 mm^2) 4H-SiC BJTs with emitter width of 40 μm .

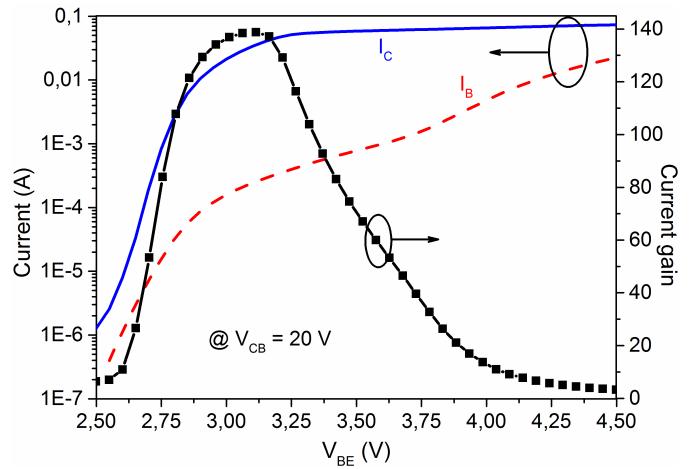


Fig. 3. Gummel plot of fabricated BJTs measured under $V_{CB} = 20 \text{ V}$.

III. RESULTS AND DISCUSSION

Fig. 2 shows the wafer-level I - V characteristics at room temperature of the fabricated BJTs with an emitter width of 40 μm . About 30% of the BJTs showed a record high current gain of ($\beta_{\max} = 139$). An ON-resistance $R_{ON} = 98 \text{ m}\Omega\cdot\text{cm}^2$ was measured at about 10 mA without considering the current spreading effect. However, in order to extract the actual R_{ON} , the active area of 0.18 mm^2 was calculated, based on the calculation method used in [5]. Therefore, the ON-resistance was estimated to be 579 $\text{m}\Omega\cdot\text{cm}^2$. This value is lower than the drift resistance of 754 $\text{m}\Omega\cdot\text{cm}^2$ calculated with an electron mobility of 940 cm^2/Vs according to the modeling in [29]. Hence, conductivity modulation may be present. However, an efficient lifetime enhancement procedure is needed after the drift layer growth to achieve a complete conductivity modulation [30]. The open-base breakdown voltage (BV_{CEO}) was measured whereas the wafer was submersed in dielectric silicone fluid to avoid air sparking, and the BJTs contacted by means of probe tips. The leakage current was measured about 0.025 μA (14 $\mu\text{A}/\text{cm}^2$), 0.18 μA (0.1 mA/cm^2), and 0.5 μA (0.28 mA/cm^2), at the reverse voltage of 15 kV, 15.8 kV and 16.25 kV, respectively. Fig. 3 shows a Gummel plot of the fabricated BJTs measured

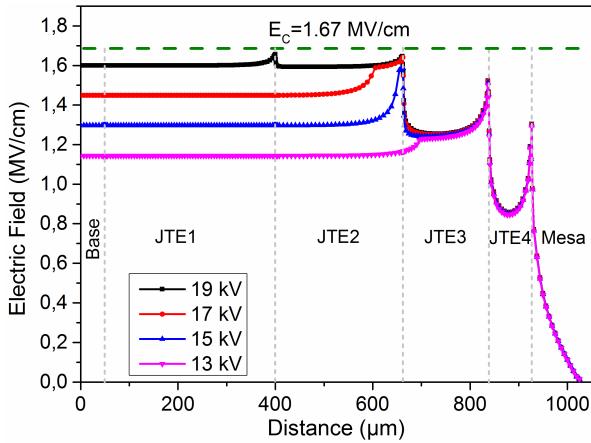


Fig. 4. The simulated electric field distribution for the O-JTE at different reverse voltages. The dashed line indicates the critical electric field for SiC according to [31].

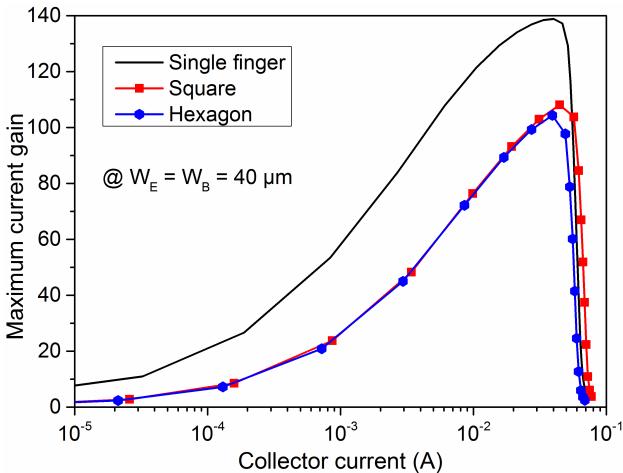


Fig. 5. Current gain as a function of collector current with $W_E = W_B = 40 \mu\text{m}$ for different cell geometries under $V_{CB} = 20 \text{ V}$.

under $V_{CB} = 20 \text{ V}$. A maximum current gain of 139 was achieved at $V_{BE} = 3.15 \text{ V}$ which is in a good agreement with the ON-state characteristics in Fig. 2.

Fig. 4 shows a comparison of the electric field distribution along the AB cut line in Fig. 1 for different applied reverse voltages. It shows that the electric field distribution is uniform at 19 kV and there is no peak of the electric field at the edges.

Fig. 5 shows the maximum current gain as a function of collector current for different cell geometries measured under $V_{CB} = 20 \text{ V}$. These devices have the same base area and emitter and base widths ($W_E = W_B = 40 \mu\text{m}$). It shows that the single finger geometry has the highest β due to the smallest emitter periphery to area (P_E/A_E) ratio as discussed in [5]. The square and hexagon cell geometries have the same β because of a comparable (P_E/A_E) ratio. It also shows that at a given current gain, square and hexagon cell geometries have higher collector current due to a better utilization of the base area which confirms our previous results in [5].

Recently, we demonstrated that wider emitter ($>40 \mu\text{m}$) does not result in higher current gain due to the saturation behavior [5]. Fig. 6 shows the maximum current gain as a

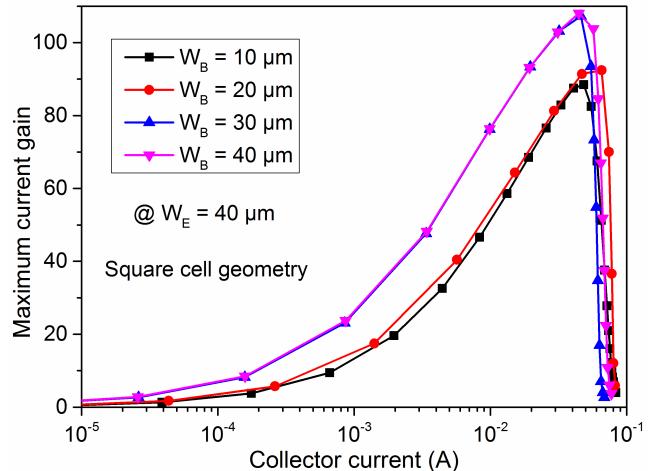


Fig. 6. Current gain as a function of collector current for square cell geometry with $W_E = 40 \mu\text{m}$ but different W_B s under $V_{CB} = 20 \text{ V}$.

function of collector current for square cell geometry and different base widths. The β is decreasing as the base width reduces below $30 \mu\text{m}$. It is also apparent that a wider base ($>30 \mu\text{m}$) does not result in higher current gain due to the same saturation behavior. The hexagon cell geometry has the same trend as the square cell geometry. Therefore, an emitter width of $W_E = 40 \mu\text{m}$ and base width of $W_B = 30 \mu\text{m}$ are sufficient to have a high current gain. Our observation is that wider emitter and base widths than the optimal size only increase the cost with no other improvement.

IV. CONCLUSION

Implantation-free 15-kV-class small-area (0.08 mm^2) 4H-SiC BJTs utilizing area-optimized junction termination extension (O-JTE) have been demonstrated with a record high current gain (β) of 139 and ON-resistance (R_{ON}) of $534 \text{ m}\Omega\cdot\text{cm}^2$. An open-base breakdown voltage (BV_{CEO}) of 15.8 kV at leakage current density of $0.1 \text{ mA}/\text{cm}^2$ was measured. Different cell geometries (single finger, square, and hexagon) have been compared. The base size effect has been investigated. These results show that too wide emitter and base widths only consumes area and thus increases cost with no performance improvement.

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