WBGlobalSemi, Inc.

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High Power Design System with 3.3 kV, 50 A Power Module (PM) and Universal Gate Drive Amplifier with Enhanced Protection (UGDA), Sam Ochi, VP Engineering

We will enable electrical engineers & computer scientists to design & develop power electronics systems with improved in performance & protection on key metrics. Our design system consists of user CCC, power CCC, and PM to enable fastest switching for current & future WBG power devices. And while minimizing overvoltages, inadvertent faults, other switching issues, and providing the extremely fast overcurrent protection needed by these devices to achieve reliable performance in many applications.

For high V applications we can deliver faster switching, less noise, greater protection.

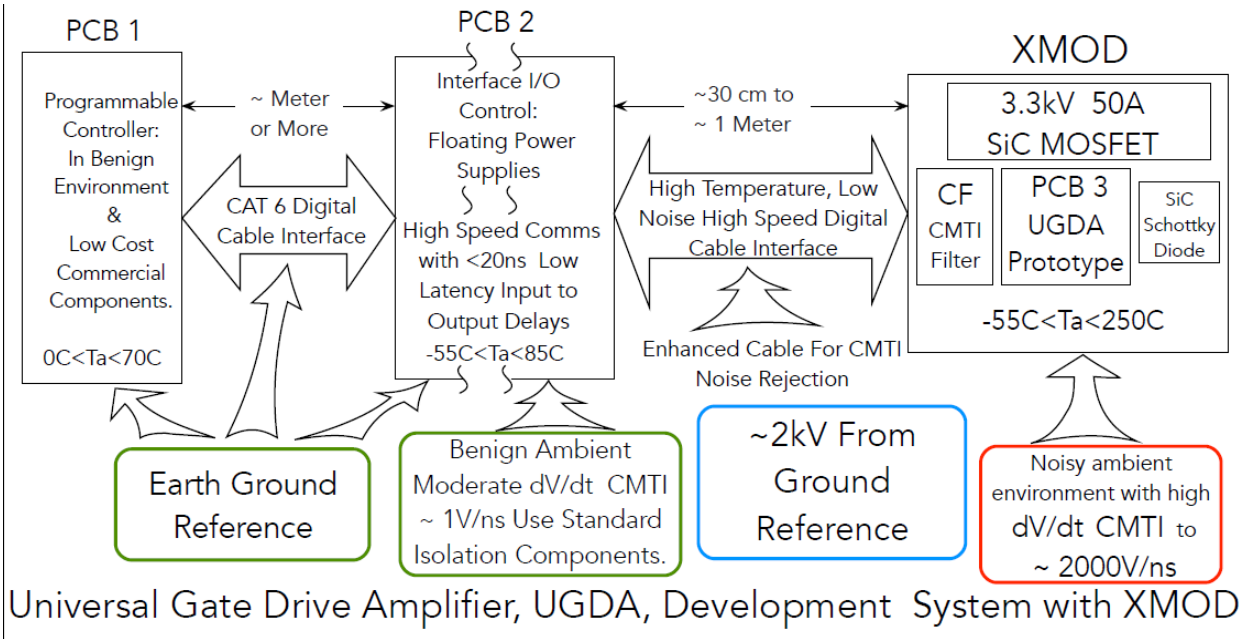
We optimize the performance & protection of SiC MOSFETS by using novel designs to achieve 3 goals:

(1) deliver high speed desaturation/overcurrent event shut down protection. We implement a fully programmable blanking circuit to prevent false noise induced triggering and a fully programmable shutdown sequence to "softly" (controlled & programmed manner) turn-off the SiC MOSFET without triggering a destructive avalanche **V(BR)DSS** breakdown. This turnoff in < 500 ns safely protects & shuts down the driven SiC MOSFET during any detected event. Current gate drives are designed for Si power semiconductors & deliver protection shut down from > 5 us to 10 us after a desaturation/overcurrent event. WBG devices operate at approximately 10X to 20X the power density of Si devices are less tolerant than Si devices and may self-destruct or be permanently damaged within 1us to 3us.

(2) safely withstand dV/dt switching noise from >200 V/ns to 1,000 V/ns. Current commercial gate drives typically deliver <150V/ns, e.g. http://www.ti.com/product/UCC21710-Q1. Our CMTI Filter (CF) circuit accepting input dV/dt of >500V/ns provide high efficiency, error free switching at the higher frequencies typical with SiC MOSFETs, reducing mass & size of decoupling capacitors and inductors used in power systems.

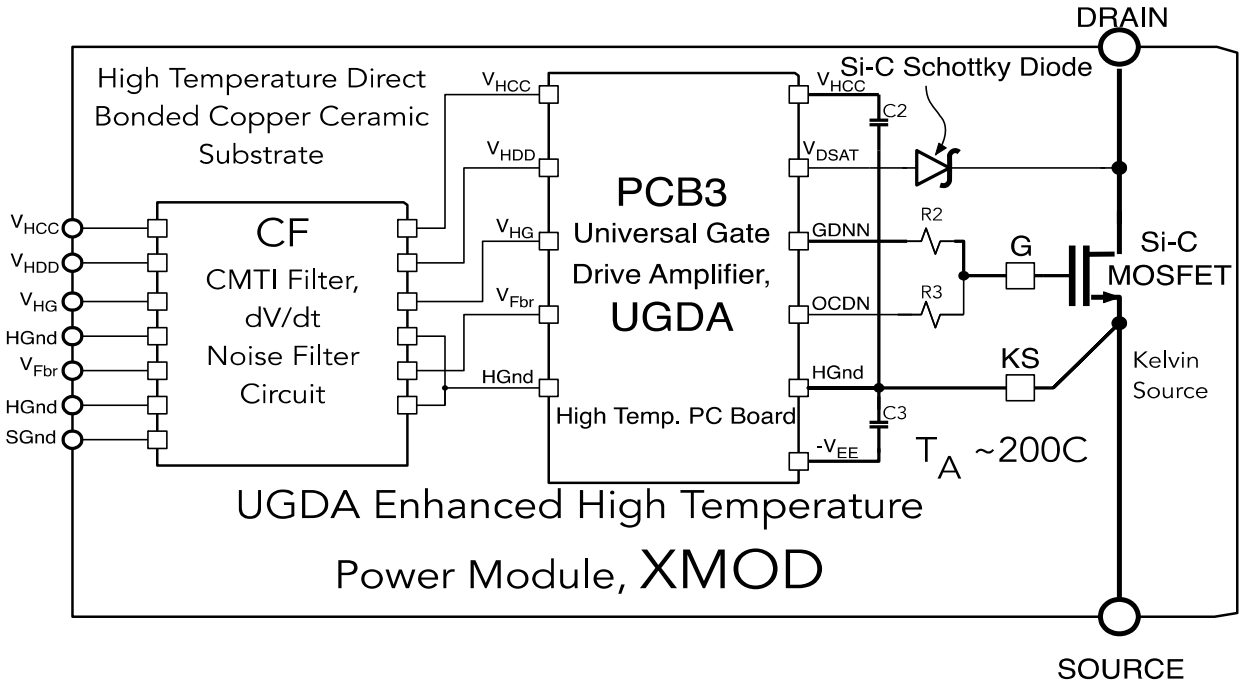
(3) improve switching behavior of a driven SiC MOSFET bare die by co-packaging a bare die gate drive in a PM. Key improvements in switching behavior include reduced rise time, **tr**, reduced fall time, **tf**, as well as reduced gate to source voltage overshoot or undershoot, **VGS**. These reductions improve overall system efficiency & SiC MOSFET in circuit reliability so the PM improves power converter performance.

Table 1 (over) identifies our targets. First our MBs enables transient noise immunity >500V/ns, is substantial higher than highest available commercial gate driver system. Second, our overcurrent comparator's output, **VFBAR** can provide overcurrent error output back to the controller in < 20ns maximum from the PM.



This feature allows power control techniques such as adaptive dead time control for high power - with potential to reducing power loss by 12% in voltage based converters. Third our UGDA + PM does not require a daughter board on top of the power module to reduce inductance, where the least heat tolerant component limits the SiC MOSFET performance! Our technology road map includes a future SiC gate drive semiconductor and components to enable an all SiC PM for high temperature performance.

Phase 1 Technical Goals of Universal Gate Driver Amplifier With SiC MOSFET (50A 3.3KV) and Desaturation/Overcurrent Protection					
Parameter	**Conditions** (Unless Otherwise, V_{HCC}=20V, $-V_{EE}$=-5V)	**Min**	**Typ**	**Max**	**Units**
Common Mode Transient Immunity, CMTI	CF, CMTI Filter, dV/dt Noise Filter Circuit Inserted	500	1000	2000	V/ns
Switching Frequency Range, f_{sw}		1		200	Khz
Input to Ouptut Delays, t_d			50	70	ns
Rise Time, t_r	Gate Drive Amplifier Driving C_{LD}=4nF, R2=2Ω			20	ns
Fall Time, t_f				20	ns
Desaturation/Overcurrent Detection Threshold, V_{DSTH}	Internally Programmable		10		V
Diode Clamp Voltage Set, V_{DSAT}	Internally Programmable		18		V
Overcurrent Comparator Delay, V_{Fbar}	From the Time when $\|V_{DSAT}-V_{DSTH}\| > \|5mV\|$			20	ns
Overcurrent "Softly" Shutdown	Externally Adjustable, R3=60Ω		400		ns
Overcurrent Blanking	Internally Programmable	100	400		ns



Sam Ochi, MSEE, WBGS VP Engineering, designed 35 gate drives and 100+ commercial analog, digital, mixed signal, and power semiconductors working at National Semi, AMD, Teledyne, Maxim, IXYS, Analog Devices, and Microsemi (now Microchip).