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10+ kV Implantation-Free 4H-SiC PiN Diodes

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Abstract. Implantation-free mesa etched 10+ kV 4H-SiC PiN diodes are fabricated, measured and analyzed by device simulation. An area-optimized junction termination extension (O-JTE) is implemented in order to achieve a high breakdown voltage. The diodes design allows a high breakdown voltage of about 19.3 kV according to simulations by Sentaurus TCAD. No breakdown voltage is recorded up to 10 kV with a very low leakage current of 0.1 μA. The current spreading within the thick drift layer is considered and a voltage drop (V_F) of 8.3 V and 11.4 V are measured at 50 A/cm^2 and 100 A/cm^2, respectively. The differential on-resistance (Diff. R_{on}) of 67.7 mΩ.cm^2 and 55.7 mΩ.cm^2 are measured at 50 A/cm^2 and 100 A/cm^2, respectively.

Introduction

Silicon carbide (SiC) is an excellent candidate for high-voltage and high-temperature applications due to its superior properties such as wide bandgap, high critical electric field, and high thermal conductivity [1], [2]. 4H-SiC up to 1.7 kV unipolar devices are now commercially available. However, future advanced electric power networks need ultra-high-voltage (> 10 kV) devices with low-loss [3]. Bipolar devices such as PiN diodes have the advantage of reduced On-resistance (R_{On}) compared with unipolar devices. Table 1 summarizes recent results reported for ultra-high-voltage 4H-SiC PiN diodes.

In order to achieve a high blocking voltage (BV), an efficient and manufacturable junction termination is needed. Ion implantation followed by high-temperature annealing to activate the implanted dopants is commonly utilized to form the termination. A disadvantage with ion implantation is that the implanted area can get lifetime killer defects resulting in bipolar degradation [4]. Furthermore, ultra-high-voltage devices require a large area termination which increases the cost. Recently, we presented an implantation-free optimized termination junction termination extension (O-JTE) with a high efficiency about 92 % [5]. In this type of termination, the number of zones, length, and dose of each zone is optimized in order to achieve a high breakdown voltage with an optimized area termination [6], [7]. In this work, we present a 10+ kV implantation-free 4H-SiC test PiN diode utilizing O-JTE. The 2-D device simulation Sentaurus TCAD was utilized in order to achieve a high breakdown voltage with an optimized area termination.

Table 1. Performance comparison between ultra-high-voltage 4H-SiC PiN diodes diodes.

BV (kV)	V_F (V) @ 100A/cm^2	R_{ON} (mΩ·cm^2)	Growth	Ref. / Size [a.]
10	3.87	38	off-axis	[8] / L
>10	3.3	3.4	on-axis	[9] / S
10-13	3.75	3.3	off-axis	[10] / L
15	4.1	25.5	off-axis	[11] / L
10+ kV	8.3 @ 50A/cm^2 11.4 @ 100A/cm^2	67.7 @ 50A/cm^2 55.7 @ 100A/cm^2	off-axis	This work / S
21.7	9.34 @ 50A/cm^2	63.4 @ 50A/cm^2	off-axis	[12]/ L

[a.] "S" for small-area (<0.5 mm^2) low-current (<1 A) and "L" for large-area (>2.5 mm^2) high-current (>5 A).

Device Structure and Fabrication

Fig. 1 shows a cross-sectional view of a fabricated circular test PiN diode with a 100 µm diameter (active area = 65×10^{-3} mm^2) for the anode. The diode has a punch-through design, hence an 8 µm n-type buffer layer was grown and doped to 1.1×10^{16} cm^{-3} on a 100 mm 4° off-axis 4H-SiC substrate. A 125 µm thick n$^-$ drift layer was grown and nitrogen doped in situ to 1.1×10^{14} cm^{-3}. The wafer was polished by chemical mechanical polishing (CMP) to improve the surface morphology. The p-layer was subsequently grown to 700 nm aluminum doped to 2.5×10^{17} cm^{-3}. An O-JTE with descending length structure of the JTE zones applied to achieve a uniform electric field distribution and a lower peak electric field. Three main parameters; the number of the JTE zones, their etching depth, and their lengths were optimized to achieve the optimum design (see Table 2). Reactive ion etching (RIE) with a photoresist mask was utilized to form a well-controlled four-zone etched JTE. Inductively coupled plasma (ICP) etching with an oxide mask was used to form the mesa.

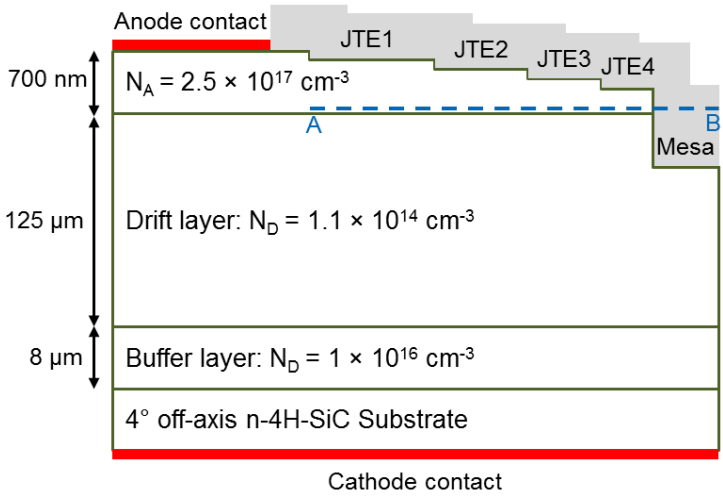

Fig. 1. Schematic cross-sectional view of the fabricated 4H-SiC PiN diodes with the O-JTE.

A dry sacrificial oxidation process was done for 3 hours at 1100 °C to reduce the surface defects caused by the etching steps in accordance to [13]. In order to minimize the interface charges at the SiO_2/SiC interface, a surface passivation was grown with 100-nm PECVD deposited SiO_2 followed by annealing in N_2O ambient at 1250 °C for 1 hour [14]. A 140-nm Ni layer was deposited as a cathode and followed by rapid thermal annealing (RTA) at 950 °C for 1 min in N_2 ambient to form the ohmic n-contact. An 110-nm stack layer of Ni/Ti/Al with the thickness ratio of 0.1/0.15/0.85 was deposited for the anode contacts followed by RTA at 850 °C for 90 sec in Ar ambient. A 500-nm Al was sputtered and formed on the anode in order to improve the current spreading. Subsequently, 2.5 µm thick SiO_2 was deposited by PECVD. The windows were opened in the oxide and a 3-µm Al was sputtered and formed on the anode. Finally, a 450-nm metal stack consisting of TiW/Ni/Au with the thickness ratio of 0.1/0.7/0.2 was sputtered for the cathode contact.

Results and Discussion

Fig. 2 shows the measured *I-V* forward characteristics of the fabricated PiN diodes at room temperature. The extracted ideality factor of $\eta = 1.52$ indicates generation-recombination due to the deep levels in the bandgap. In order to calculate the voltage drop (V_F) and differential on-resistance (Diff. R_{on}), current spreading was considered within the thick drift layer. The V_F of 8.3 V and 11.4 V were measured at 50 A/cm^2 and 100 A/cm^2, respectively. The V_F could be improved by increasing the lifetime. Similarly, the Diff. R_{on} of 67.7 mΩ.cm^2 and 55.7 mΩ.cm^2 were measured at 50 A/cm^2 and 100 A/cm^2, respectively. Utilizing the TLM structures the anode contact resistivity and the intrinsic p-layer sheet resistance were extracted to 1.8×10^{-3} Ω.cm^2 and 37.7 kΩ /sq., respectively. The anode contact resistivity can be improved by implementing a thin and high doped cap layer for the anode. Although this improvement may result in a slightly better performance, the on-resistance of the diode is so close to the drift resistance.

Table 2. The length and etch depth of the O-JTE

Zone	JTE1	JTE2	JTE3	JTE4	Mesa
Etch depth	260 nm	80 nm	80 nm	120 nm	1.5 µm
Length	350 µm	263 µm	175 µm	87 mm	25 µm

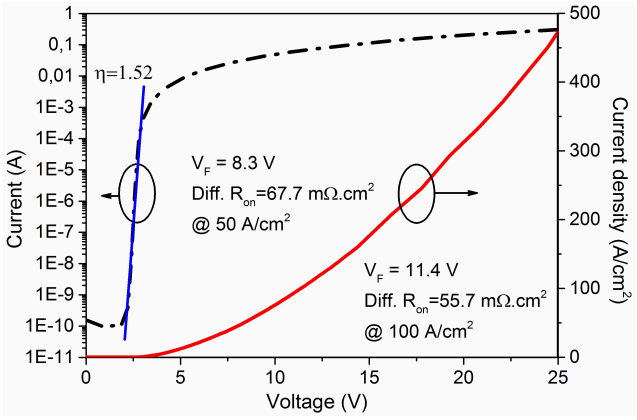

Fig. 2. Measured *I-V* forward characteristics of a fabricated test PiN diode, shown with logarithmic (left) and linear (right) scales.

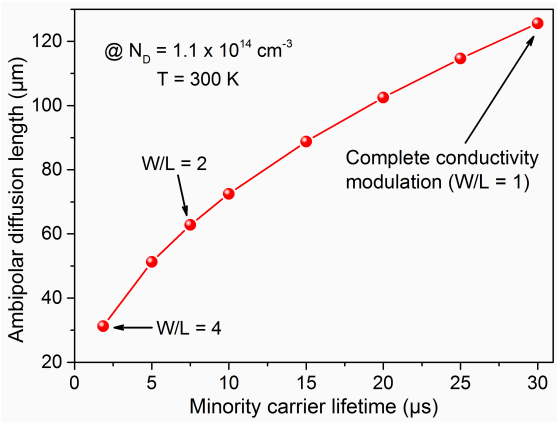

Fig. 3. Calculated ambipolar diffusion length (L) versus minority carrier lifetime (τ_p).

The ohmic resistance of the non-modulated drift layer is calculated based on equation (1) as below:

$$R=W/q\mu_n n_0 = 754\ m\Omega.cm^2 \quad (1)$$

where W, q, μ_n, and n_0, are the drift thickness, the charge of the electron, electron mobility (μ_n = 940 cm^2/Vs according to the modeling in [15]), and doping concentration of the drift layer, respectively. It shows that the drift region is conductivity modulated. A further investigation of conductivity modulation could be done by studying the ambipolar diffusion length (L) given by:

$$L = (D\tau_p)^{0.5} \quad (2)$$

$$D = 2Dpb / (b+1) \quad (3)$$

$$Dp = kT\ \mu_p / q \quad (4)$$

$$b = \mu_n / \mu_p \quad (5)$$

where D, τ_p, Dp, k, T, and μ_p are ambipolar diffusion coefficient, minority carrier lifetime, hole diffusion coefficient, Boltzmann constant, temperature, and hole mobility, respectively. Fig. 3 shows the calculated ambipolar diffusion length as a function of minority carrier lifetime. As lifetime increases, the ambipolar diffusion length raises which results in a better degree of modulation (W/L). A complete conductivity modulation (W/L = 1) of the drift region requires a minority carrier lifetime of (τ_p = 30 μs).

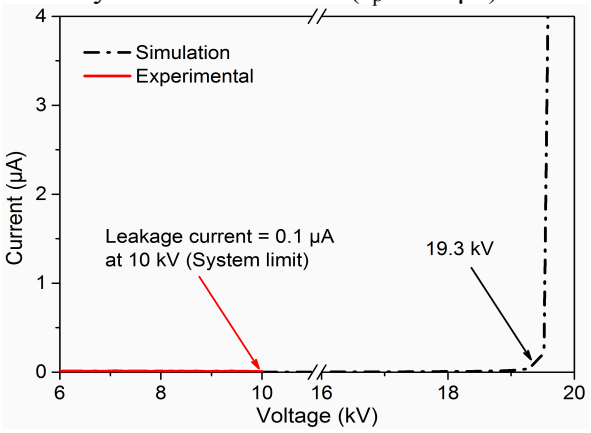

Fig. 4. Measured and simulated reverse characteristics of the fabricated PiN diodes at room temperature.

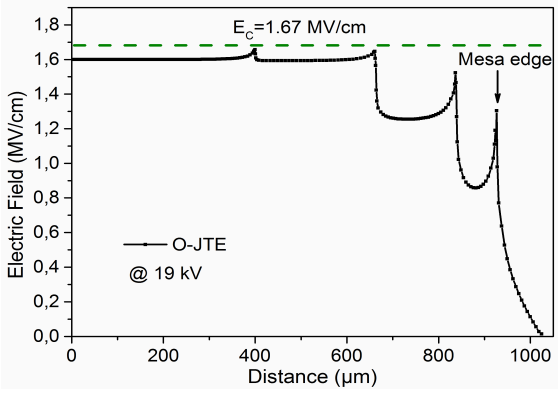

Fig. 5. Simulated electric field distribution for the O-JTE at the reverse bias of 19.3 kV. The dashed line indicates the critical electric field for SiC according to [16].

Fig. 4 shows the measured and simulated *I-V* reverse characteristics of the fabricated PiN diodes at room temperature. The device design allows for a breakdown voltage of about 19.3 kV according to simulations by Sentaurus TCAD. No breakdown voltage was recorded up to 10 kV (our

measurement system limit at present) with a low leakage current of 0.1 μA. Fig. 5 shows the electric field distribution along the AB cut line in Fig.1 at the applied reverse voltage of 19 kV. The electric field distribution is completely uniform and there is no peak of the electric field at the edges which results in a stable breakdown voltage.

Summary

10+ kV implantation-free 4H-SiC test PiN diodes with an efficient and area-optimized junction termination extension (O-JTE) have been fabricated. By considering the current spreading through the thick drift layer a voltage drop (V_F) of 8.3 V and 11.4 V were measured at 50 A/cm^2 and 100 A/cm^2, respectively. The differential on-resistance (Diff. R_{on}) of 67.7 mΩ.cm^2 and 55.7 mΩ.cm^2 were measured at 50 A/cm^2 and 100 A/cm^2, respectively which show the effect of conductivity modulation. No breakdown voltage was recorded up to 10 kV with a very low leakage current of 0.1 μA. A minority carrier lifetime in the drift region (125 μm, 1.1×10^{14} cm^{-3}) of τ_p = 30 μs can result in a complete conductivity modulation.

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